Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	261	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/12 14:45
L2	176	(712/235).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/12 14:45
L3	25	(branch$3 near4 (fall?through or alternate)) with decod$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/12 14:46
L4	47	(branch$3 with (fall?through or alternate)) with decod$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/12 15:25
L5	6	(branch$3 with (fall?through or alternate)) with (concurrent$2 or simulatneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/12 15:26
L6	17	(branch$3 with (fall?through or alternate)) same (concurrent$2 or simulatneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/09/12 15:26
S1	166	(712/235).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:42
S2	245	(712/237).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 08:54
S3	0	(branch$3 near4 (fall?through) near4 target) near4 decode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:35
S4	3	(branch$3 near4 (fall?through or alternate) near4 target) with decode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:36
S5	14	(branch$3 with (fall?through or alternate) with target) with decode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:12
S6	141	(branch$3 adj1 unit$1) near4 (decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:12

S7	2	(branch$3 adj1 unit$1) near4 (decod$3) near4 cycle$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:33
S8	1	("5961637").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:32
S9	3	((branch$3 adj1 unit$1) near4 (decod$3)) with cycle$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:33
S10	0	((branch$3 adj1 unit$1) near4 (decod$3)) same (("same" or equal) adj1 cycle)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:34
S11	18	((branch$3 adj1 unit$1) near4 (decod$3)) same cycle$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:34
S12	0	(branch$3 near4 (fall?through)) near4 decode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:35
S13	3	(branch$3 near4 (fall?through)) with decod$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:35
S14	25	(branch$3 near4 (fall?through or alternate)) with decod$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2004/12/16 09:36

Terms used
branch fall through parallel or **concurrent** or **simulatneous**

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1 Concurrent garbage collection using hardware-assisted profiling

Timothy H. Heil, James E. Smith

October 2000 **ACM SIGPLAN Notices , Proceedings of the 2nd international symposium on Memory management**, Volume 36 Issue 1

Full text available: pdf(1.74 MB) Additional Information: full citation, abstract, citings, index terms

In the presence of on-chip multithreading, a Virtual Machine (VM) implementation can readily take advantage of *service threads* for enhancing performance by performing tasks such as profile collection and analysis, dynamic optimization, and garbage collection concurrently with program execution. In this context, a hardware-assisted profiling mechanism is proposed. The *Relational Profiling Architecture* (RPA) is designed from the top down. RPA is based on a relational model similar ...

2 Techniques for debugging parallel programs with flowback analysis

Jong-Deok Choi, Barton P. Miller, Robert H. B. Netzer

October 1991 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 13 Issue 4

Full text available: pdf(2.73 MB) Additional Information: full citation, references, citings, index terms

Keywords: debugging, flowback analysis, incremental tracing, parallel program, program dependence graph, semantic analysis

3 Critical path reduction for scalar programs

Michael Schlansker, Vinod Kathail

December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(1.38 MB) Additional Information: full citation, references, citings, index terms

4 Obtaining sequential efficiency for concurrent object-oriented languages

John Plevyak, Xingbin Zhang, Andrew A. Chien

January 1995 **Proceedings of the 22nd ACM SIGPLAN-SIGACT symposium on Principles of programming languages**

Full text available: pdf(1.09 MB) Additional Information: full citation, abstract, references, citings, index terms

Concurrent object-oriented programming (COOP) languages focus the abstraction and encapsulation power of abstract data types on the problem of concurrency control. In

Terms used
branch sequential parallel or **concurrent** or **simulatneous**

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1 Tutorial: Compiling concurrent languages for sequential processors

Stephen A. Edwards

April 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 2

Full text available: pdf(771.65 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Embedded systems often include a traditional processor capable of executing sequential code, but both control and data-dominated tasks are often more naturally expressed using one of the many domain-specific concurrent specification languages. This article surveys a variety of techniques for translating these concurrent specifications into sequential code. The techniques address compiling a wide variety of languages, ranging from dataflow to Petri nets. Each uses a different method, to some degr ...

Keywords: Compilation, Esterel, Lustre, Petri nets, Verilog, code generation, communication, concurrency, dataflow, discrete-event, partial evaluation, sequential

2 Parallel execution of prolog programs: a survey

Gopal Gupta, Enrico Pontelli, Khayri A.M. Ali, Mats Carlsson, Manuel V. Hermenegildo

July 2001 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 23 Issue 4

Full text available: pdf(1.95 MB) Additional Information: full citation, abstract, references, citings, index terms

Since the early days of logic programming, researchers in the field realized the potential for exploitation of parallelism present in the execution of logic programs. Their high-level nature, the presence of nondeterminism, and their referential transparency, among other characteristics, make logic programs interesting candidates for obtaining speedups through parallel execution. At the same time, the fact that the typical applications of logic programming frequently involve irregular computatio ...

Keywords: Automatic parallelization, constraint programming, logic programming, parallelism, prolog

3 Parallel logic programming systems

Jacques Chassin de Kergommeaux, Philippe Codognet

September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3

Full text available: pdf(3.51 MB) Additional Information: full citation, abstract, references, citings, index terms

Terms used
branch target sequential parallel or **concurrent** or **simulatneous**

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1 Tutorial: Compiling concurrent languages for sequential processors
Stephen A. Edwards
April 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 2

Full text available: pdf(771.65 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Embedded systems often include a traditional processor capable of executing sequential code, but both control and data-dominated tasks are often more naturally expressed using one of the many domain-specific concurrent specification languages. This article surveys a variety of techniques for translating these concurrent specifications into sequential code. The techniques address compiling a wide variety of languages, ranging from dataflow to Petri nets. Each uses a different method, to some degr ...

Keywords: Compilation, Esterel, Lustre, Petri nets, Verilog, code generation, communication, concurrency, dataflow, discrete-event, partial evaluation, sequential

2 Parallel logic programming systems
Jacques Chassin de Kergommeaux, Philippe Codognet
September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3

Full text available: pdf(3.51 MB) Additional Information: full citation, abstract, references, citings, index terms

Parallelizing logic programming has attracted much interest in the research community, because of the intrinsic OR- and AND-parallelisms of logic programs. One research stream aims at transparent exploitation of parallelism in existing logic programming languages such as Prolog, while the family of concurrent logic languages develops language constructs allowing programmers to express the concurrency—that is, the communication and synchronization between parallel processes—withi ...

Keywords: AND-parallelism, OR-parallelism, Prolog, Warren Abstract Machine, binding arrays, concurrent constraint programming, constraints, guard, hash windows, load balancing, massive parallelism, memory management, multisequential implementation techniques, nondeterminism, scheduling parallel tasks, static analysis

3 Parallel execution of prolog programs: a survey
Gopal Gupta, Enrico Pontelli, Khayri A.M. Ali, Mats Carlsson, Manuel V. Hermenegildo
July 2001 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 23 Issue 4

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#3	((branch <paragraph> (sequential <or> fall-through) <paragraph> target <paragraph> (concurrently <or> parallel <or> simultaneously))<in>metadata)	4

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Scholar Results **1** - **9** of **9** for **branch** + (**sequential** or **fall-through**) + **target** + (**concurrent** or **simultaneous** or **parallel**).

EPIC: An Architecture for Instruction-Level **Parallel** Processors
MS Schlansker, BR Rau - HP Laboratories Palo Alto, HPL-1999-111, February, 2000 - users.ece.gatech.edu
... to do so and what the **target** address is ... require efficient static schedules for **branch**-intensive loop ... implementation of a **sequential** architecture must cope with ...
Cited by 27 - View as HTML - Web Search - eecs.umich.edu - ece.uc.edu - hpl.hp.com - all 15 versions »

[PS] A Communication Layer for the Embedded Heterogeneous Multi-Processor **Target** of the Spar Compiler
S Cadot - pds.twi.tudelft.nl
... Vnus program **sequential** ... of the DMA-based communication hardware of the embedded **target**, the ensemble ... such as load/store, floating-point, and **branch**) can only ...
View as HTML - Web Search

Delft University of Technology **Parallel** and Distributed Systems Report Series
S Cadot, K Langendoen, C van Reeuwijk - pds.ewi.tudelft.nl
... Vnus program **sequential** ... of the DMA-based communication hardware of the embedded **target**, the ensemble ... such as load/store, floating-point, and **branch**) can only ...
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Support for Software Assisted Speculative Execution
EC Lewis - cis.upenn.edu
... speculatively executed in **parallel** if the **branch** is predicted to **fall through**. ... with the **sequential** register file at the root ... register file per **branch**, or n total ...
View as HTML - Web Search - cs.washington.edu - cis.upenn.edu

A high-level abstraction of shared accesses
PJ Keleher - ACM Transactions on Computer Systems, 2000 - portal.acm.org
... protocols. SDSM protocols support the abstraction of shared memory to **parallel** applications running on networks of worksta- Author ...
Cited by 5 - Web Search - motefs.cs.umd.edu - cs.umd.edu - x1.cs.umd.edu - all 5 versions »

Implementation of H-PAM
S Cadot, K Langendoen, HJ Sips, C van Reeuwijk - pds.twi.tudelft.nl
... by the mapper program, which transforms **sequential** Vnus code ... hardware of the embedded **target**, the ensemble ... 0.841471f) { /* the Athlon will execute this **branch** ...
View as HTML - Web Search - joses.pds.twi.tudelft.nl

Worst Case Execution Time Estimation for Advanced Processor Architectures
L fur Realzeit–Computersysteme - deposit.ddb.de
... the control transfer instructions is introduced and fed into a **branch** predictor model ... These tokens have source and **target** dependencies to model the register and ...
View as HTML - Web Search - tumb1.biblio.tu-muenchen.de - cs.york.ac.uk - www-users.cs.york.ac.uk

Abstracts of papers presented during the 51 stAnnual Conference of The Anatomical Society of India, ...
NAS PROSPECTIVE, POFM NERVE - J. Anat. Soc. India, 2004 - medind.nic.in
... Interestingly, this **branch** joined the median nerve forming ... This presentation is aimed at this **target** group. ... **CONCURRENT** ANOMALIES OF RIGHT RENAL VEIN AND RIGHT ...
View as HTML - Web Search - medind.nic.in

Web Results 1 - 10 of about 272 for branch + (sequential or fall-through) + target + (concurrent or simultaneous or para

Scholarly articles for **branch + (sequential or fall-through) + target + (concurrent or simultaneous or parallel)**

EPIC: An Architecture for Instruction-Level Parallel ... - by Schlansker - 27 citations
A Communication Layer for the Embedded Heterogeneous ... - by Cadot - 0 citations
Delft University of Technology Parallel and Distributed ... - by Cadot - 0 citations

US Patent Class 712-- ELECTRICAL COMPUTERS AND DIGITAL PROCESSING ...
Sequential. 9, DF .~.~.~ **Concurrent**. 10, DF .~ Array processor ... **Simultaneous parallel** fetching or executing of both **branch** and **fall-through** path ...
www.patentec.com/data/class/712.html - 16k - Cached - Similar pages

[PDF] 5 10 15 20 25 30 35 CLASS 712 ELECTRICAL COMPUTERS AND DIGITAL ...
File Format: PDF/Adobe Acrobat - View as HTML
Vector processor operation. 8 ...**Sequential**. 9 ...**Concurrent** .Array processor ... **Simultaneous parallel** fetching. or executing of both **branch** ...
www.uspto.gov/go/classification/uspc712/sched712.pdf - Similar pages

Class Schedule for Class 712 ELECTRICAL COMPUTERS AND DIGITAL ...
... level is 3 **Simultaneous parallel** fetching or executing of both **branch** ...
Subclass 237 indent level is 3 Prefetching a **branch target** (ie, look ahead) ...
www.uspto.gov/go/classification/uspc712/sched712.htm - 81k - Sep 11, 2005 - Cached - Similar pages
[More results from www.uspto.gov]

Patent 4833599: Hierarchical priority **branch** handling for **parallel** ...
... a global controller for determining a **fall-through** program counter ... codes can be used in **branch** determination. ... that ultimately force code to be made **sequential**. ...
freepatentsonline.com/4833599.html - 101k - Supplemental Result - Cached - Similar pages

Manual of Classification
... multichip or multimodule processor having **sequential** program control. ... executing of both **branch** and **fall-through** path. ... Prefetching a **branch target** (ie, look ahead ...
www.ipatent.net/classdef/MANUAL/class712/span.html - 33k - Supplemental Result - Cached - Similar pages

[PDF] Using Dynamic **Branch** Behavior for Power-Efficient Instruction Fetch
File Format: PDF/Adobe Acrobat
By avoiding this **simultaneous** accesses, **sequential**. trace caches (STC)achieve lower power ... whose **target/fall-through** instruction leads to the creation of ...
doi.ieeecomputersociety.org/10.1109/ISVLSI.2003.1183363 - Similar pages

[PDF] Trace Cache: a Low Latency Approach to High Bandwidth Instruction ...
File Format: PDF/Adobe Acrobat
branch in the trace is predicted taken. The trace cache is accessed in **parallel** with the instruction ... **Branch target** and **fall-through** addresses are filled ...
doi.ieeecomputersociety.org/10.1109/MICRO.1996.566447 - Similar pages

UNIFICATION OF SYNCHRONOUS AND ASYNCHRONOUS MODELS FOR **PARALLEL** ...
Another problem arises when the **target** of a **branch** is located inside of a ...
Concurrent C processes are **sequential** in nature, and follow directly the ...
dynamo.ecn.purdue.edu/~hankd/CARP/XPC/paper.html - 200k - Cached - Similar pages

[PS] Instruction Fetch Mechanisms for Multipath Execution Processors ...
File Format: Adobe PostScript - View as Text